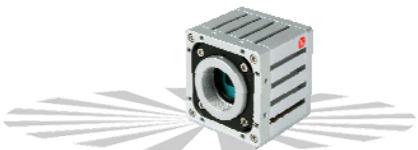
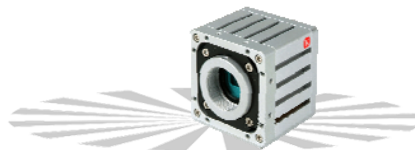
HDC3 Camera Platform

Concept, design, functions, projects



Overview
HDC3 Platform

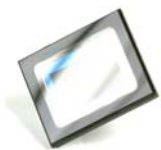
- HDC3 is a development platform for customer-specific products
- Based on the following main components
  - Global Shutter Sony Pregius© CMOS Sensoren
  - FPGA (Altera Cyclone V) based signal processing
  - External microcontroller (STM32) for control loops and control interface
  - HD-SDI output
  - Customer-specific power supply
- Ruggedized Design
- Platform for the development of cameras for regulated areas (e.g., aviation or automotive)



CMOS Sensor

Sony Pregius ©

- Global Shutter – 3 generations (3 complementary series)
  e.g.: 5,86 µm pixel with 2,35 Mpixel
  e.g..: 3,45 µm pixel with 5,087 Mpixel
  e.g.: 4,5 µm pixel with 2,8 Mpixel
- Up to 48 dB gain
  (24 dB analog and 24 dB digital)
- Exposure time adjustable in the line raster
  t_{min} in 1080p mode approx. 43 µs @ 30 fps and 28.5 µs @ 60 fps
- Horizontal and vertical image mirror
- Various readout modes (1080p, ROI, …)
  Bracketing support (WDR mode)



Signal Processing

- Color interpolation and color correction
- White balance (automatic, manual, presets)
- Gamma correction
- Edge enhancement (unsharp masking)
- Histogram-based contrast stretching, optional global histogram equalization (HDRadapt)
- Line generator
- Exposure and gain control
- Adjustable measurement windows for controls

Signal Output

HD-SDI

- Standardized image formats and frame rates
- Digital data transfer over coax cable
  YCbCr 4:2:2 format with 8 or 10 bit
- Continuous video stream
  extern Sync possible
- SMPTE259M – SD-SDI (optional in connection with analog PAL/NTSC)
  270 Mbit/s (13.5 MHz pixel clock)
  digital transmission of image data with 720x576x50i (PAL) or 720x484x60i (NTSC) resolution
- SMPTE292M – HD-SDI
  1.485 Gbit/s (74.25 MHz pixel clock)
  Digital transmission of image data up to 720p60, 1080p30 and 1080i60
- SMPTE424M – 3G-SDI
  2.97 Gbit/s (148.5 MHz pixel clock)
  Digital transmission of image data up to 1080p60

Control

Camera based on HDC3 platform

- Control of camera parameters via RS232 or RS485
- Register / value-based parametrization
  Protocol modeled on Genicam GenCP
  (e.g., addressing of serveral cameras at an RS485 master, error detection, synchronization of data transfer)

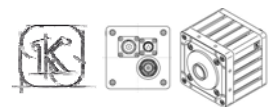
Options
Customizing

Sensor-ROI
Integrated image memory enables shiftable ROI 720p or 1080p ROI, e.g., for optical alignment
Scaling enables emulation of active areas if cameras have to be replaced

Signal processing
Customer-specific functions (e.g., additional image statistics, meta data, frame accumulation, event mark)
HDR/WDR mode

Inputs/ outputs:
Additional analog PAL/NTSC video output
External synchronization

Camera control:
Discrete in- and outputs for control of camera functions (e.g., event mark) and status display (e.g., BIT status)
CAN-Bus instead of RS232/RS485 or additional
Customer-specific RS232/RS485 protocol



Standard development vs dvelopment for regulated applications

Standard development
(Product without specific requirements on development processes)

Development process following the Kappa standard
Modular system of Hardware, FPGA-firmware and µC-software for basic functionality
Adaptation to customer requirements (e.g., dependence of functions, external interfaces)

Standard development vs development for regulated applications

Development for regulated applications (e.g. aviation or automotive)

Development process is specified by external standards, e.g., DO178C/DO254 (aviation) or ISO26262 (automotive)

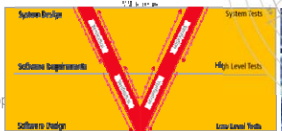
- Requirements documents (system, hardware, software, …) and design standards (e.g., MISRA C coding standard)
- Creation of design documents
- Implementation (hardware, source code, …) and integration
- Verification (sometimes very extensive, e.g., additional unit tests for software)
- Milestones and reviews prescribed by the standard

The effort required depends on the required design assurance level

- Requirements-based development with traceability of requirements sometimes down to the circuit or source code
- Modular system can be used at best as copy template only (because of traceability, dead code, test effort)

Major restrictions for the use of standard components (e.g., bought-in IP cores)




Products and projects based on the HDC3 platform

- Tauri 3.0 / 3.1
  - Camera with IMX252LQR,1080p30 format and standard functions for Kappa
- Project periscope camera (sea, military)
  - Customer-specific system with IMX174LQR and 1080p25 format
  - Customer-specific interfaces and functions (frame accumulation, image statistics, meta data, WDR function)
- Project head-up display camera (aviation, military)
  - Customer-specific development based on IMX273LQR and 720p60 format
  - Customer-specific interfaces and functions (event mark, BIT state, reduced standard functionality)
  - Development according to DO178C software level D and DO254 DAL D
- Project rearview mirror replacement (automotive)
  - Customer-specific system consisting of camera (IMX252LQR) and display with 720p60 format
  - Customer-specific interfaces (CAN, APIX2, motorized lens)
  - Development according to ISO26262 ASIL-B